UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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MARSHALL, GERSTEIN & BORUN LLP
233 S. WACKER DRIVE, SUITE 6300
SEARS TOWER
CHICAGO, IL 60606

EXAMINER
MOORE, PATRICK M

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/749,425	SUBRAMONEY ET AL.
	Examiner	Art Unit	
	Patrick M. Moore	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>31 December 2003</u>.

2a)☐ This action is **FINAL.** 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-21</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-21</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date <u>6/16/05 & 5/27/04</u>.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

DETAILED ACTION

1. Claims 1-21 have been examined.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 27 May 2004 and 16 June

2005 were considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 8-15, 18 & 19 are rejected under 35 U.S.C. 102(b) as being anticipated

by Campbell (US Patent #6,393,522).

a. **As per Claim 1**, Campbell discloses an article comprising a machine-accessible

medium **[Figure 1, #106, #107 & #108]** having stored thereon instructions that,

when executed by a machine, cause the machine to: obtain, from a performance

monitor, performance data for a memory heap having a plurality of memory

regions **[Figure 4, #403, #404, #407 & Column 2, Lines 24-36]**; based on the

performance data, determine if at least one of the plurality memory regions is a

delinquent region **[Figure 4, #405 & Column 2, Lines 24-36]**; and in response to

a determination that at least one of the plurality of memory regions is a

delinquent region, execute a memory management routine to optimize that

region of the memory heap **[Column 2, Line 66 – Column 3, Line 5]**. *Examiner*

understands that cache eviction, as disclosed by Campbell, is a memory

management routine that optimizes memory regions.

b. **As per Claim 2**, Campbell further discloses the article of claim 1, wherein the

performance data represents at least one memory performance event **[Column**

2, Lines 11-13].

c. **As per Claim 3**, Campbell further discloses the article of claim 1, wherein the

performance data is selected from the group consisting of cache misses,

translation lookaside buffer misses, branch mis-predicts, stalls due to data

dependency, and data cache write-back **[Column 2, Lines 14-36]**. *Using the*

definition of cache miss, Examiner understands that performance data are

inherently anticipated by the system taught by Campbell.

d. **As per Claim 4**, Campbell further discloses the article of claim 1, wherein the

performance monitor is a Performance Monitoring Unit (PMU) **[Figure 1, #105]**.

e. **As per Claim 5**, Campbell further discloses the article of claim 1, having further

instructions that, when executed by the machine, cause the machine to: execute

the memory management routine on at least one delinquent region; and execute

a secondary memory management routine on at least one non-delinquent region,

wherein the secondary memory management routine is different than the

memory management routine **[Column 2, Line 66 – Column 3, Line 5]**. *The*

delinquent regions are evicted from the cache, while the non-delinquent regions

are not evicted and may have additional 'decision process[es]' performed..

f. **As per Claim 8**, Campbell further discloses the article of claim 1, having further instructions that, when executed by the machine, cause the machine to: establish a size granularity of the memory region prior to obtaining the performance data for the memory region **[Column 3, Lines 47-54]**.

g. **As per Claim 9**, Campbell further discloses the article of claim 1, wherein the performance data is received from a Performance Monitoring Unit, having further instructions that, when executed by the machine, cause the Performance Monitoring Unit to: count the number of occurrences of the performance data **[Column 2, Lines 53-55]**.

h. **As per Claim 10**, Campbell further discloses the article of claim 9, having further instructions that, when executed by the machine, cause the Performance Monitoring Unit to: compare the count of the number of occurrences of the performance data to a threshold value **[Column 2, Lines 24-36]**, wherein if the count is above the threshold value, a delinquent region is determined to exist **[Column 2, Lines 56-59]**.

i. **As per Claim 11**, Campbell further discloses the article of claim 10, having further instructions that when executed by the machine, cause the machine to: determine if a sufficient number of data samples have been taken, before comparing the count to the threshold value **[Figure 4, #408 & Column 2, Lines 60-65]**.

j. **As per Claim 12**, Campbell further discloses the article of claim 10, having further instructions that, when executed by the machine, cause the machine to: in

response to a determination that an additional data sample is to be taken, collect
the additional data sample from the memory heap **[Column 4, Lines 28-34]**.

k. **As per Claim 13**, Campbell further discloses the article of claim 1, having further
instructions that, when executed by the machine, cause the machine to: block the
delinquent region from memory storage **[Column 2, Line 66 – Column 3, Line
5]**. *As is well known in the art, Examiner understands that the term 'evicted', as
taught by Campbell, refers to blocking access requests to the referenced
memory location.*

l. **As per Claim 14**, Campbell discloses a method comprising: identifying load miss
memory addresses from a memory heap including a plurality of memory regions
[Figure 1, #106, #107 & #108]; maintaining a frequency count for the identified
load miss memory addresses **[Figure 1, #104 & Column 2, Lines 24-36]**;
determining if any of the plurality of memory regions include a threshold value of
load miss memory addresses **[Column 2, Lines 56-59]**; and optimizing the
memory heap in response to a determination that at least one of the plurality of
memory regions includes a threshold value of load miss memory addresses
[Column 2, Line 66 – Column 3, Line 5].

m. **As per Claim 15**, Campbell further discloses the method of claim 14, wherein
optimizing the memory heap comprises blocking the memory regions including
the threshold value of load miss memory addresses **['evicted' entry in Column
2, Line 66 – Column 3, Line 5]**.

n. **As per Claim 18**, Campbell further discloses the method of claim 14, further

comprising: performing a first memory management routine on at least one

memory region including the threshold value of load miss memory addresses;

and performing a second memory management routine, different than the first

memory management routine, on at least one memory region that does not

include the threshold value of load miss memory addresses **[Column 2, Line 66**

– Column 3, Line 5].

o. **As per Claim 19**, Campbell discloses a system comprising: hardware to monitor

performance of a memory heap and to compile performance data on memory

regions within the memory heap **[Figure 1, #105, #104 & Column 3, Lines 16-**

37], wherein the hardware is able to determine if any of the memory regions are

delinquent regions based on the compiled performance data **[Column 2, Lines**

24-36]; and a memory manager for optimizing the delinquent regions **[Figure 1,**

#105 & Column 2, Line 66 – Column 3, Line 5].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 7, 16, 17, 20 & 21 are rejected under 35 U.S.C. 103(a) as being

unpatentable over **Campbell** (US Patent # 6,393,522) as applied to Claims 1, 14 & 19

above, and further in view of Chilimbi et al.'s "Using Generational Garbage Collection to Implement Cache-Conscious Data Placement", herein **Chilimbi A**.

a. **Campbell** *does not expressly disclose the delinquent memory management routine as a garbage collector. However,* **Chilimbi A** *discloses several garbage collection routines.* **Campbell** *and* **Chilimbi A** *are analogous art because they are from the same field of endeavor: increasing operational performance of cache memory systems. At the time of invention, it would have been obvious for one of ordinary skill in the art to combine the Cache Memory Management system, as disclosed by* **Campbell***, with the Garbage Collection techniques, as disclosed by* **Chilimbi A***. The suggestion/motivation for doing so would have been for the benefit of increasing the overall cache response speed by applying a dynamic reorganization of cached data as taught by* **Chilimbi A** *on* **Section 2, ¶4,** *which spans* **Pages 1 & 2.**

b. **As per Claim 6, Chilimbi A** further discloses the article of claim 1, having further instructions that, when executed by the machine, cause the machine to: execute a garbage collection routine on at least one delinquent region **[Section 2, ¶4].**

c. **As per Claim 16, Chilimbi A** further discloses the method of claim 14, wherein optimizing the memory heap comprises performing a garbage collection on at least one of the memory regions including the threshold value of load miss memory addresses **[Section 2, ¶4].**

d. **As per Claim 20, Campbell** discloses the system of claim 19, wherein the hardware comprises a performance monitoring unit **[Figure 1, #105]**, and

Chilimbi A discloses that the memory manager is a garbage collector **[Section 2, ¶4]**.

e. **As per Claim 7, 17 & 21, Chilimbi A** further discloses the system of claim 6, 16 and 20, respectively, wherein the garbage collector executes a garbage collection optimization selected from the group consisting of reference counting collection, copy collection, generational collection, mark-sweep collection, beltway collection, oldest first collection, slide compaction or a hybrid collection **[Section 3]**. *Examiner understands that* **Chilimbi A** *discloses several distinct optimization techniques, which include generational, copying, breadth-first, oldest first, reference counting collection, etc. Additionally, it would be inherent to apply additional algorithms or to use several algorithms in combination. Identical motivation to combine* **Campbell** *with* **Chilimbi A** *exists, as above.*

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick M. Moore whose telephone number is (571) 272-1239. The examiner can normally be reached on M-F 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabahn can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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published applications may be obtained from either Private PAIR or Public PAIR.

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

PMM

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER